Seavo Motherboard
User's Manual
用户手册

SV1a-64126 Series

Ver 0.0

SEAVO 信 | 步 | 科 | 技 |
中国物联网设备主板领导者

Contents

1.Models and Attentions

1.1 Models

This manual is applied to following models:

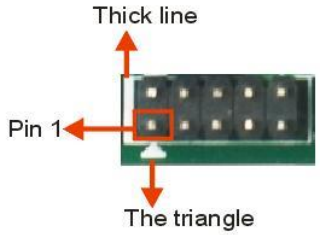
Model	CPU	COM	LAN	USB	HDMI	eDP1/LVDS	eDP2	M.2 Key-M	M.2 Key-E	M.2 Key-B	SATA 3.0
SV1a-64126	J6412	6	2	11	1	LVDS	1	SATA	WIFI+BT	4G/5G	1

1.2 Attentions

1) **Notes under a table or figure indicate the difference of models, or alternative definition of specific pin of the header (jumper/connector).**

2) **How to identify the first pin of a header or jumper**

- Usually, there is a thick line or a triangle near the header's or jumper's pin 1.



- Square pad, which you can find on the back of the motherboard, is usually used for pin 1.

2.Specification

Model	SV1a-64126
CPU	Intel® Celeron® J6412, Quad-core, clock speed 2.00 GHz, up to 2.60GHz, TDP 10W
Display	1 * HDMI (TYPE-A): max resolution up to 4096x2160@30Hz 1 * eDP1/LVDS (Header): LVDS max resolution up to 1920x1200@60Hz (default) or eDP max resolution up to 4096*2160@60Hz 1 * eDP2 [1] (Header): eDP max resolution up to 4096*2160@60Hz
Memory	Support DDR4-2666/2933/3200MHz, 1 * non-ECC SO-DIMM Slot, Up to 32GB
Storage	1 * SATA3.0 7P Connector (With 1 * SATA Power Header) 1 * M.2 (NGFF) Key-M Slot (SATA SSD, 2242/2260/2280) [2]
Ethernet	RJ45_1: 1 * Realtek GBE LAN Chip (RJ45, 10/100/1000 Mbps) RJ45_2: 1 * Realtek GBE LAN Chip (RJ45, 10/100/1000 Mbps) [3]
Audio	Realtek ALC662 5.1 Channel HDA Codec (USB Audio Codec optional [4]), 1 * Line-Out + MIC 2in1 3.5mm Jack (Default CTIA, OMTP standard sel by res) 1 * Front Audio Header (Line-Out + MIC) 2 * Amplifier Header, 5-W (per channel) into an 8-Ω Loads
Expansion Slots	1 * M.2 (NGFF) Key-E Slot (PCIE+USB2.0, Support WIFI+BT, 2230) 1 * M.2 (NGFF) Key-B Slot [5] (3042/3052, PCIE [2]+ USB2.0 [6], Support 4G/5G, With 1 * SIM Card Header)
COM	1 * RS232 (COM1, DB9/M, Full Lanes) [1][7] 1 * RS232/RS485 (COM2, Header, Full Lanes) 1 * RS232/TTL (COM3, Header, Full Lanes) 3 * RS232 (COM4/5/6, Header, Full Lanes)
USB	4 * USB3.0 (TYPE-A, Rear IO) [5] 7 * USB2.0 (Header, Internal) [3][4][6]
Other Ports	1 * GPIO Header 1 * Front Panel Header (HDD LED+PWR LED+PWR-ON+RESET) 1 * Cash Drawer Header 1 * ESPI Header 1 * System FAN Header 1 * CPU FAN Header 1 * Case Open Header 2 * Debug Header 1 * CMOS Clear Jumper 1 * AT or ATX Select Jumper 1 * ME Flash Jumper
System	Windows 10 64-bit, Linux
Temperature	Storage: -20~75℃ Operating: 0~60℃
BIOS	AMI UEFI BIOS (Support Watchdog Timer)

Power Supply	DC 12V 1 * DC 12V Power Input Φ2.5mm Jack [8] 1 * DC 12V Power Input Header 1 * DC 12V + 5V Power Output Header
Factor	ITX Standard (170mm * 170mm)

Notes:

[1]: HDMI2 and EDP2 share the same signal, they cannot be accessed simultaneously. HDMI2 colay with COM1(DB9M) on the same position. Support EDP2 and COM1 by default.

[2]: M.2_KEYB_SSD1 can support PCIe x2/ SATA SSD, selectable by BOM. Support SATA SSD by default. (If M.2_KEYB_WWAN1 supports PCIE, M.2_KEYB_SSD1 only supports SATA SSD.)

[3]: R_USB1 and F_USB1 share the same signal, they cannot be accessed simultaneously. R_USB1 colay with RJ45_2 on the same position. Support F_USB1 and RJ45_2 by default.

[4]: F_USB5 colay USB2_9 signal with USB audio codec. It supports F_USB5 by default and can support USB audio codec if specified. (resistor selectable)

[5]: M.2_KEYB_WWAN1 colay USB3_3 signal with R_USB2. It supports R_USB2 by default and can support M.2_KEYB_WWAN1 if specified. (resistor selectable)

[6]: F_USB4 colay USB2_4 signal with M.2_KEYB_WWAN1. It supports M.2_KEYB_WWAN1 by default and can support F_USB4 if specified. (resistor selectable)

[7]: COM1(DB9M) and J_COM1(Header) share the same signal, they cannot be accessed simultaneously. Support COM1(DB9M) by default.

[8]: DC 12V Power Input Mini-din 4P Jack optional.

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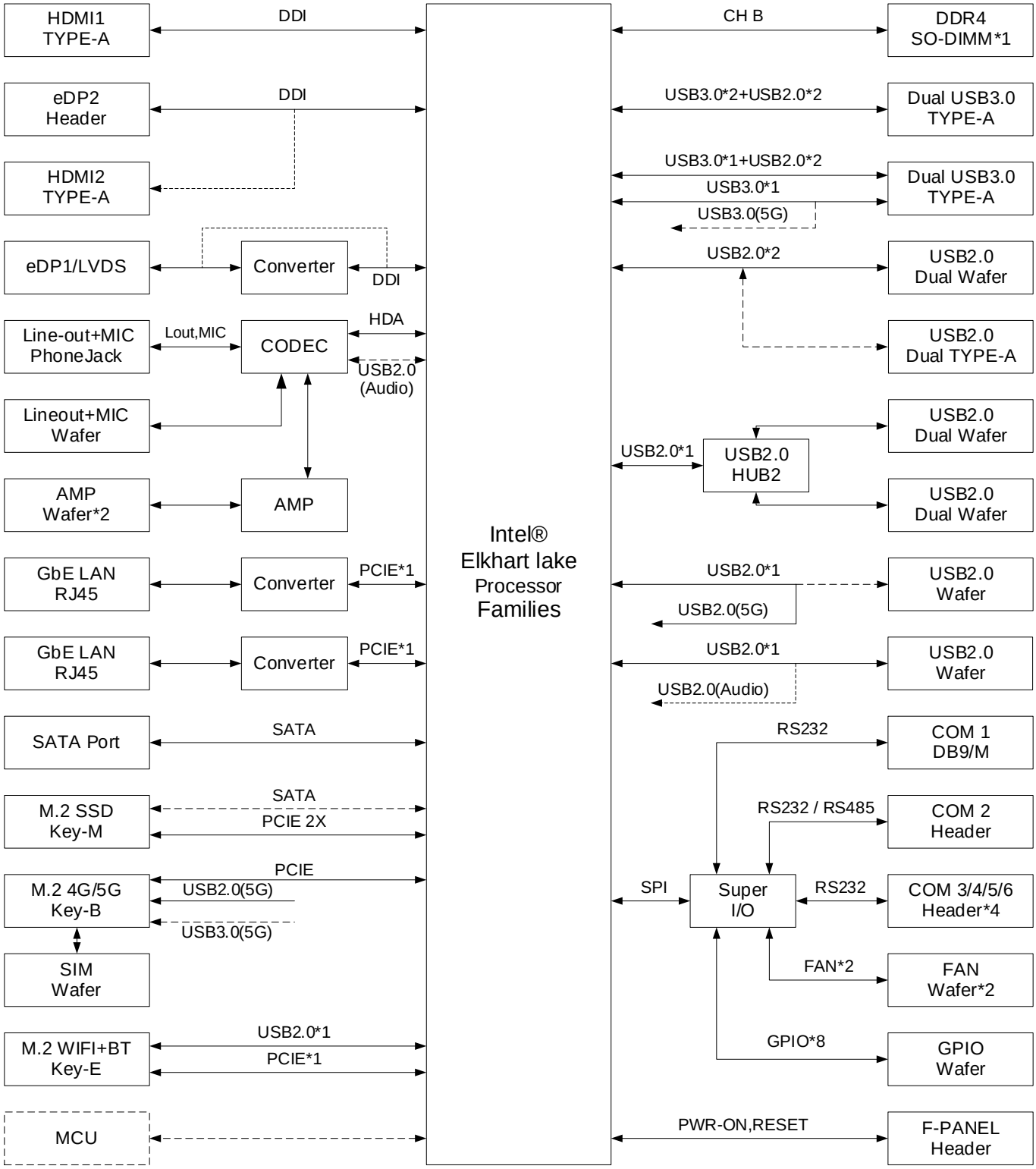
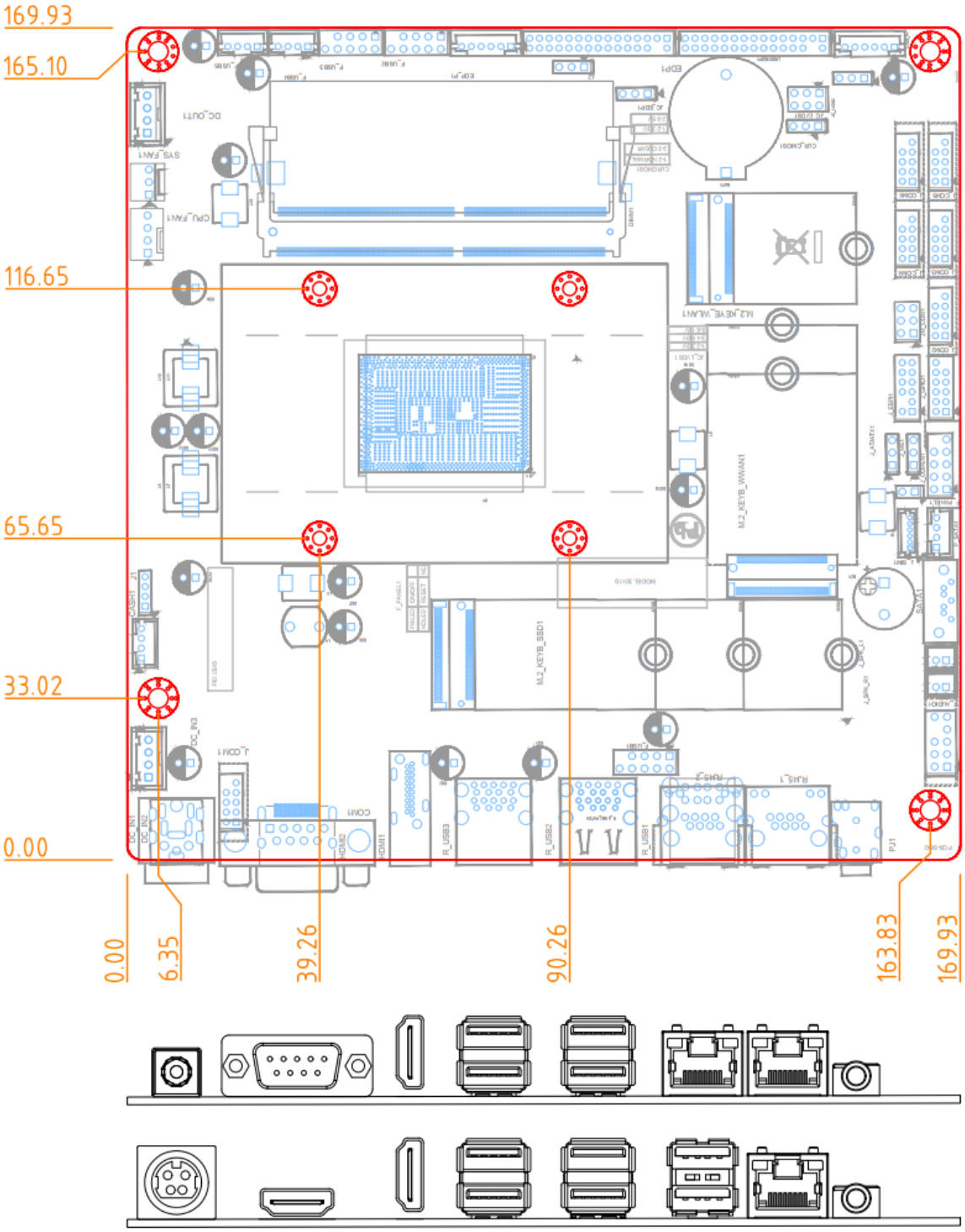
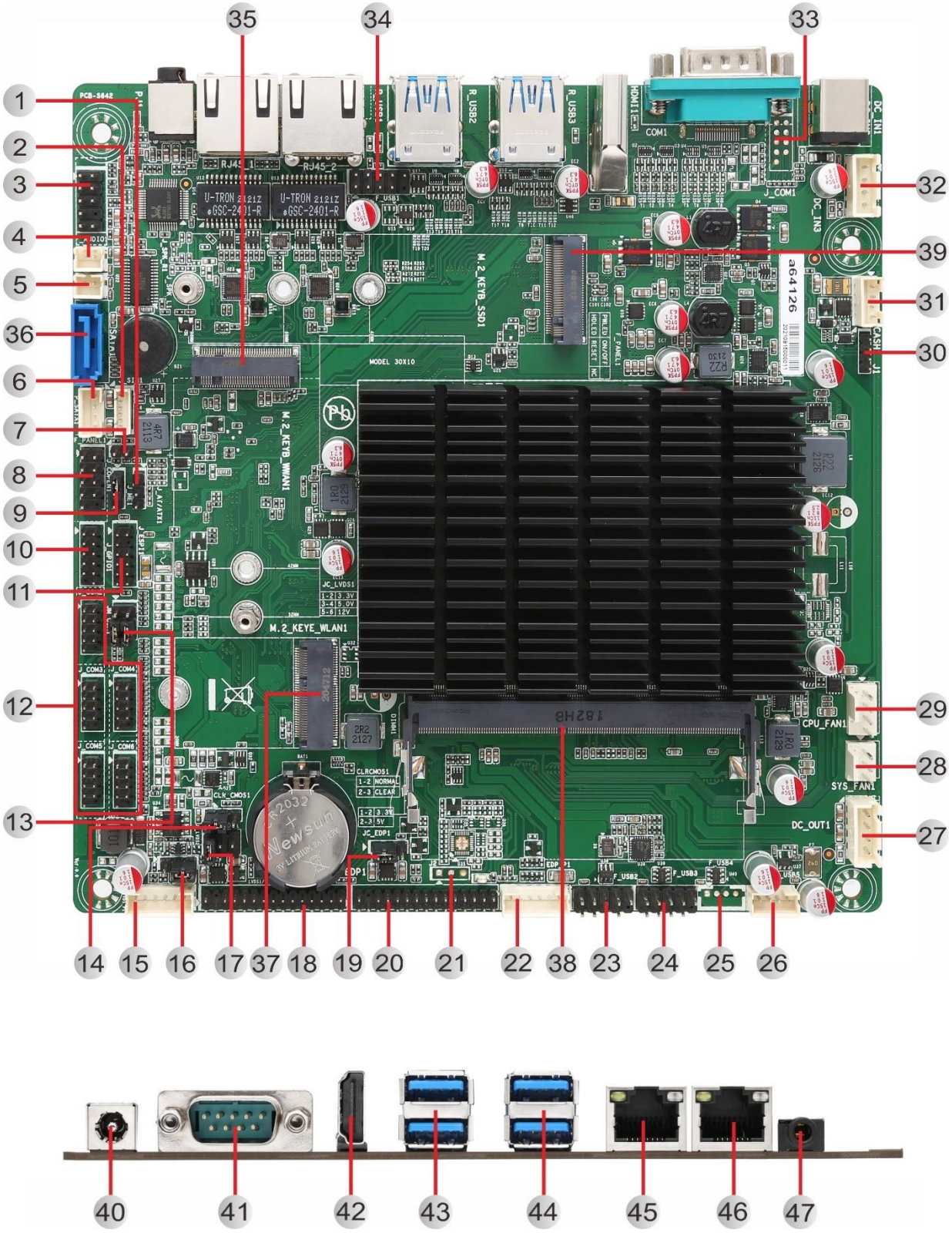
3.Functional Block Diagram



4. Mechanical Drawing



5. Jumpers / Headers and Connectors



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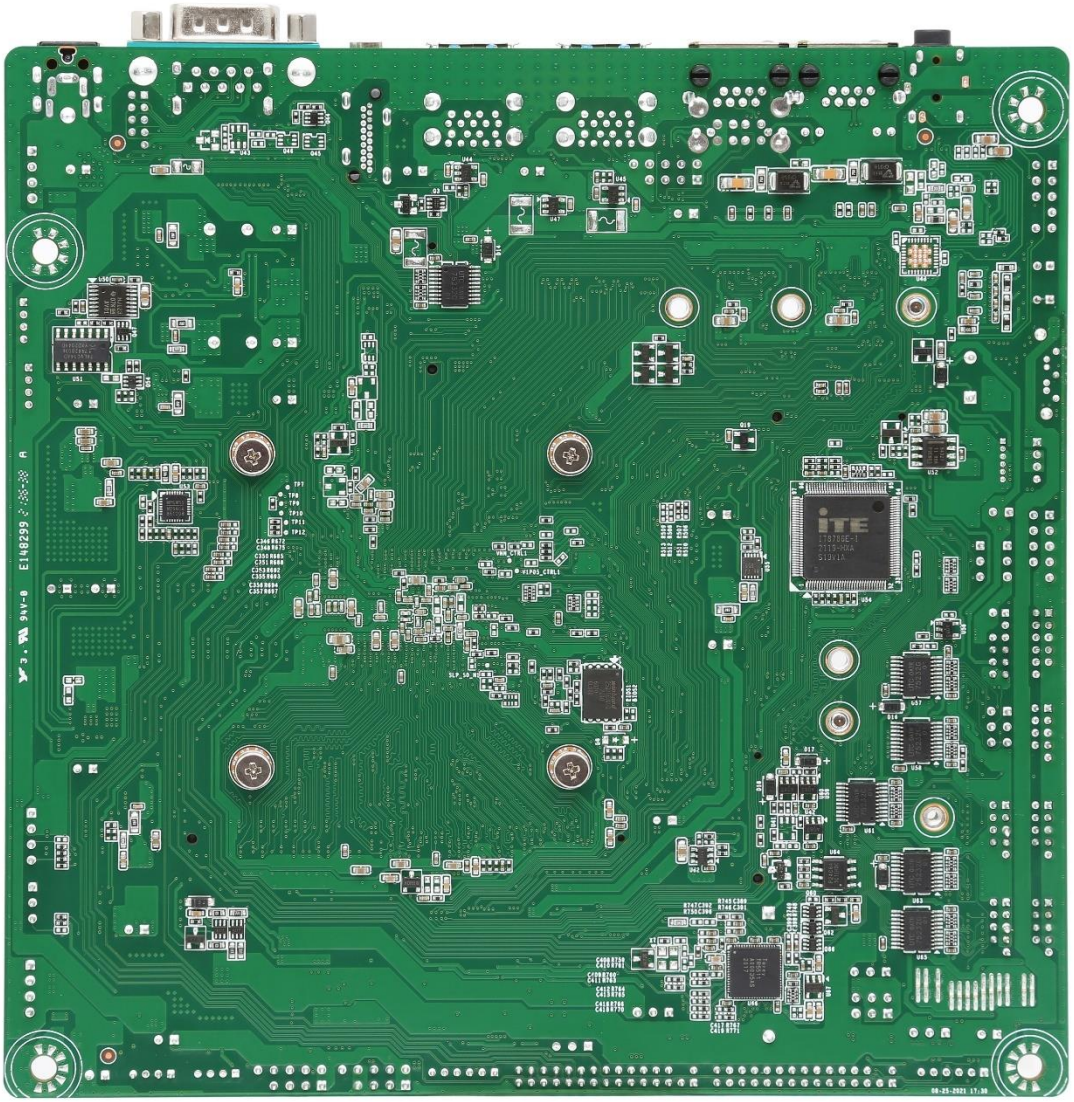

Jumpers / Headers and Connectors		
1	J_AT/ATX1	AT or ATX Select Jumper
2	J_SIM1	SIM Card Header
3	F_AUDIO1	Front Audio Header (Line-Out + MIC)
4	J_SPK_R1	Right Amplifier Header
5	J_SPK_L1	Left Amplifier Header
6	P_SATA1	SATA Power Header
7	J_COPEN1	Case Open Header
8	F_PANEL1	Front Panel Header
9	J_ME1	ME Flash Jumper
10	J_GPIO1	GPIO Header
11	J_ESPI1	ESPI Header
12	J_COM2/3/4/5/6	COM2/3/4/5/6 Header
13	JM_COM1	COM2 RS232/485 Select Jumper
14	CLR_CMOS1	CMOS Clear Jumper
15	LVDS_P1	eDP1/LVDS Backlight Control Header
16	JC_LVDS2	eDP1/LVDS Backlight PWM/PWM#/CCFL Select Jumper
17	JC_LVDS1	eDP1/LVDS VDD Select Jumper
18	LVDS1/EDP1	eDP1/LVDS Signal Header
19	JC_EDP1	eDP2 VDD Select Jumper
20	EDP1	eDP2 Signal Header
21	J2	Debug Header2
22	EDP_P1	eDP2 Backlight Control Header
23	F_USB2	Front USB2.0 Header2
24	F_USB3	Front USB2.0 Header3
25	F_USB4	Front USB2.0 Header4
26	F_USB5	Front USB2.0 Header5
27	DC_OUT1	DC 12V+5V Power Output Header
28	SYS_FAN1	System FAN Header
29	CPU_FAN1	CPU FAN Header
30	J1	Debug Header1
31	CASH1	Cash Drawer Header
32	DC_IN3	DC 12V Power Input Header
33	J_COM1	COM1 Header
34	F_USB1	Front USB2.0 Header1
35	M.2_KEYB_WWAN1	M.2 (NGFF) Key-B Slot (3042/3052, PCIE+USB2.0, Support 4G/5G)
36	SATA1	SATA3.0 7P Connector
37	M.2_KEYE_WLAN1	M.2 (NGFF) Key-E Slot (PCIE+USB2.0, Support WIFI+BT, 2230)
38	DIMM1	DDR4 SO-DIMM Slot
39	M.2_KEYB_SSD1	M.2 (NGFF) Key-M Slot (SATA SSD, 2242/2260/2280)

40	DC_IN2 (DC_IN1)	DC 12V Power Input Φ2.5mm Jack (DC 12V Power Input Mini-din 4P Jack optional)
41	COM1 (HDMI2)	COM1 DB9/M Connector (HDMI TYPE-A Connector optional)
42	HDMI1	HDMI Upright TYPE-A Connector
43	R_USB3	Dual USB3.0 TYPE-A Connector3
44	R_USB2	Dual USB3.0 TYPE-A Connector2
45	RJ45_2 (R_USB1)	GBE LAN RJ45 Connector2 (Dual USB3.0 TYPE-A Connector1 optional)
46	RJ45_1	GBE LAN RJ45 Connector1
47	PJ1	Line-Out + MIC 2in1 3.5mm Jack (Default CTIA, OMTP standard sel by res)

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6. Definition of Jumpers /Headers and Connectors

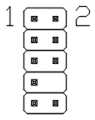
1) J_AT/ATX1 (AT or ATX Select Jumper 3*1 Pin 2.54mm)

Graphic	Setting	Function
	1-2(Default)	ATX MODE
	2-3	AT MODE

2) J_SIM1 (SIM Card Header 6*1 Pin 1.25mm)

Graphic	Pin	Definition	Pin	Definition
	1	UIM1_PWR	4	UIM1_CLK
	2	UIM1_DAT	5	UIM1_RST
	3	GND	6	UIM1_VPP

3) F_AUDIO1 (Front Audio Header (Line-Out + MIC) 5*2 Pin 2.54mm)

Graphic	Pin	Definition	Pin	Definition
	1	MIC_IN_L	2	GND
	3	MIC_IN_R	4	+ 3.3V
	5	LINE_OUT_R	6	MIC_JD
	7	GND		
	9	LINE_OUT_L	10	LINE_OUT_JD

4) J_SPK_R1 (Right Amplifier Header 2*1 Pin 2.00mm)

Graphic	Pin	Definition	Pin	Definition
	1	SPK_OUT_R-	2	SPK_OUT_R+

5) J_SPK_L1 (Left Amplifier Header 2*1 Pin 2.00mm)

Graphic	Pin	Definition	Pin	Definition
	1	SPK_OUT_L-	2	SPK_OUT_L+

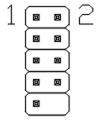
6) P_SATA1 (SATA Power Header 4*1 Pin 2.00mm)

Graphic	Pin	Definition	Pin	Definition
	1	+ 12V	3	GND
	2	GND	4	+ 5V

7) J_COPEN1 (Case Open Header 2*1 Pin 2.00mm)

Graphic	Setting	Function
	1-2: Connected	Active Case Open
	1-2: Open (Default)	Normal

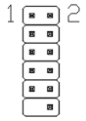
8) F_PANEL1 (Front Panel Header 5*2 Pin 2.54mm)

Graphic	Pin	Definition	Pin	Definition
	1	HDD 3.3V LED+	2	POWER 3.3V LED+
	3	HDD 3.3V LED-	4	POWER 3.3V LED-
	5	RESET-	6	POWER+
	7	RESET+	8	POWER-
	9	N/C		

9) J_ME1 (ME Flash Jumper 3*1 Pin 2.54mm)

Graphic	Setting	Function
	1-2(Default)	ME Protect
	2-3	ME Programmable

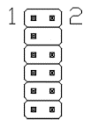
10) J_GPIO1 (GPIO Header 6*2 Pin 2.00mm)

Graphic	Pin	Definition	Pin	Definition
	1	SIO_GPI70 (0xA06 Bit0, H [1])	2	SIO_GPI71 (0xA06 Bit1, H [1])
	3	SIO_GPI72 (0xA06 Bit2, H [1])	4	SIO_GPI73 (0xA06 Bit3, H [1])
	5	GND	6	SIO_GPO74 (0xA06 Bit4, H [1])
	7	SIO_GPO75 (0xA06 Bit5, H [1])	8	SIO_GPO76 (0xA06 Bit6, H [1])
	9	SIO_GPO77 (0xA06 Bit7, H [1])	10	+ 5V
			12	N/C

Notes:

[1]: “H” or “L” means the default voltage is High or Low level (5V GPIO).

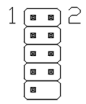
11) J_ESPI1 (ESPI Header 6*2 Pin 2.00mm)

Graphic	Pin	Definition	Pin	Definition
	1	ESPI_IO0_SIO	2	+ 3.3V
	3	ESPI_IO1_SIO		
	5	ESPI_IO2_SIO	6	ESPI_CLK_SIO
	7	ESPI_IO3_SIO	8	GND
	9	ESPI_CS0_N	10	+ 3.3V
	11	ESPI_ALERT0_N	12	ESPI_RST0_N/ BUF_PLT_RST_N [1]

Notes:

[1]: Support BUF_PLT_RST_N by default, ESPI_RST0_N optional.

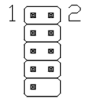
12) J_COM2/3/4/5/6 (COM2/3/4/5/6 Header 5*2 Pin 2.00mm)

Graphic	Pin	Definition	Pin	Definition
 J_COM2	1	COM2_PIN1 [1] [2]	2	COM2_PIN2 [1]
	3	COM2_TXD	4	COM2_DTR#
	5	GND	6	COM2_DSR#
	7	COM2_RTS#	8	COM2_CTS#
	9	COM2_PIN9 [3]		

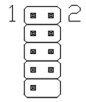
Notes:

[1]: COM2 can be RS232 (default) / RS485 selecting by “COM2 RS232/RS485 Select Jumper”. (JM_COM1 Location 13).

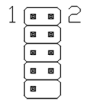
[2]: PIN1 of COM2 can be DCD# (default) /5V/12V, selectable by resistor.
[3]: PIN9 of COM2 can be RI# (default) /5V/12V, selectable by resistor.

Graphic	Pin	Definition	Pin	Definition
 J_COM3	1	COM3_PIN1 [1]	2	COM3_PIN2 [2]
	3	COM3_PIN3 [2]	4	COM3_DTR#
	5	GND	6	COM3_PIN6 [3]
	7	COM3_RTS#	8	COM3_PIN8 [2]
	9	COM3_PIN9 [2]		

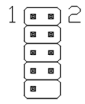
Notes:
[1]: PIN1 of COM3 can be DCD# (default) /5V/12V, selectable by resistor.
[2]: PIN2/3/8/9 of COM3 can be RS232 (default) /TTL, selectable by resistor.
[3]: PIN6 of COM3 can be DSR# (default) /3.3V/5V, selectable by resistor.

Graphic	Pin	Definition	Pin	Definition
 J_COM4	1	COM4_PIN1 [1]	2	COM4_RXD
	3	COM4_TXD	4	COM4_DTR#
	5	GND	6	COM4_DSR#
	7	COM4_RTS#	8	COM4_CTS#
	9	COM4_PIN9 [2]		

Notes:
[1]: PIN1 of COM4 can be DCD# (default) /5V/12V, selectable by resistor.
[2]: PIN9 of COM4 can be RI# (default) /5V/12V, selectable by resistor.

Graphic	Pin	Definition	Pin	Definition
 J_COM5	1	COM5_PIN1 [1]	2	COM5_RXD
	3	COM5_TXD	4	COM5_DTR#
	5	GND	6	COM5_DSR#
	7	COM5_RTS#	8	COM5_CTS#
	9	COM5_PIN9 [2]		

Notes:
[1]: PIN1 of COM5 can be DCD# (default) /5V, selectable by resistor.
[2]: PIN9 of COM5 can be RI# (default) /12V, selectable by resistor.

Graphic	Pin	Definition	Pin	Definition
 J_COM6	1	COM6_PIN1 [1]	2	COM6_RXD
	3	COM6_TXD	4	COM6_DTR#
	5	GND	6	COM6_DSR#
	7	COM6_RTS#	8	COM6_CTS#
	9	COM6_PIN9 [2]		

Notes:

[1]: PIN1 of COM6 can be DCD# (default) /5V, selectable by resistor.
[2]: PIN9 of COM6 can be RI# (default) /12V, selectable by resistor.

13) JM_COM1 (COM2 RS232/485 Select Jumper 3*2 Pin 2.54 mm)

Graphic	Setting	Function
	1-3, 2-4	COM2: RS485 (COM2_PIN1: RS485- COM2_PIN2: RS485+)
	3-5, 4-6(Default)	COM2: RS232 (COM2_PIN1: DCD# COM2_PIN2: RXD)

14) CLR_CMOS1 (CMOS Clear Jumper 3*1 Pin 2.54mm)

Graphic	Setting	Function
	1-2(Default)	Normal
	2-3	Clear CMOS

15) LVDS_P1 (eDP1/LVDS Backlight Control Header 6*1 Pin 2.00mm)

Graphic	Pin	Definition	Pin	Definition
	1	GND	4	LVDS_BKLT_EN
	2	GND	5	+ 12V
	3	LVDS_BKLT_CTL [1]	6	+ 12V

Notes:

[1]: LVDS_BKLT can be controlled by PWM(Default) /PWM#/CCFL, selectable by “eDP1/LVDS Backlight PWM/PWM#/CCFL Select Jumper”. (JC_LVDS2, Location 16).

16) JC_LVDS2 (eDP1/LVDS Backlight PWM/PWM#/CCFL Select Jumper 3*1 Pin 2.54mm)

Graphic	Setting	Function
	1-2	Controlled by PWM
	2-3(Default)	Controlled by PWM# [1]

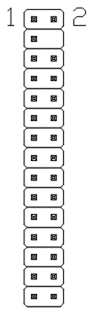
Notes:

[1]: Controlled by PWM# by default, CCFL optional. (resistor selectable)

17) JC_LVDS1 (eDP1/LVDS VDD Select Jumper 3*2 Pin 2.54 mm)

Graphic	Setting	Function
	1-2(Default)	+ 3.3V
	3-4	+ 5V
	5-6	+ 12V

18) LVDS1/EDP1 (eDP1/LVDS Signal Header 15*2 Pin 2.00mm)

Graphic	Pin	Definition	Pin	Definition
	1	VDD_PANEL [1]	2	VDD_PANEL [1]
	3	VDD_PANEL [1]		
	5	LVDS_HPD/ EDP1_HPD [2]	6	LVDS_HPD/ EDP1_HPD [2]
	7	LVDS_A_DATA0-/ N/C [2]	8	LVDS_A_DATA0+/ N/C [2]
	9	LVDS_A_DATA1-/ N/C [2]	10	LVDS_A_DATA1+/ N/C [2]
	11	LVDS_A_DATA2-/ N/C [2]	12	LVDS_A_DATA2+/ N/C [2]
	13	GND	14	GND
	15	LVDS_A_CLK-/ N/C [2]	16	LVDS_A_CLK+/ N/C [2]
	17	LVDS_A_DATA3-/ N/C [2]	18	LVDS_A_DATA3+/ N/C [2]
	19	LVDS_B_DATA0-/ EDP1_TX0- [2]	20	LVDS_B_DATA0+/ EDP1_TX0+ [2]
	21	LVDS_B_DATA1-/ EDP1_TX1- [2]	22	LVDS_B_DATA1+/ EDP1_TX1+ [2]
	23	LVDS_B_DATA2-/ EDP1_TX2- [2]	24	LVDS_B_DATA2+/ EDP1_TX2+ [2]
	25	GND	26	GND
	27	LVDS_B_CLK-/	28	LVDS_B_CLK+/

		EDP1_TX3- [2]		EDP1_TX3+ [2]
	29	LVDS_B_DATA3-/ EDP1_AUX- [2]	30	LVDS_B_DATA3+/ EDP1_AUX+ [2]

Notes:

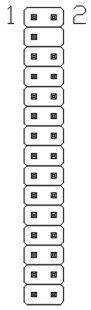
[1]: Panel Power VDD is 3.3V by default, 5V/12V is selectable by “eDP1/LVDS VDD Select Jumper” (JC_LVDS2, Table 17).

[2]: It supports LVDS by default and can support eDP if specified. (resistor selectable)

19) JC_EDP1 (eDP2 VDD Select Jumper 3*1 Pin 2.54mm)

Graphic	Setting	Function
	1-2(Default)	+ 3.3V
	2-3	+ 5V

20) EDP1 (eDP2 Signal Header 15*2 Pin 2.00mm)

Graphic	Pin	Definition	Pin	Definition
	1	VDD_PANEL2	2	VDD_PANEL2
	3	VDD_PANEL2		
	5	EDP2_HPD	6	EDP2_HPD
	7	N/C	8	N/C
	9	N/C	10	N/C
	11	N/C	12	N/C
	13	GND	14	GND
	15	N/C	16	N/C
	17	N/C	18	N/C
	19	EDP2_TX0-	20	EDP2_TX0+
	21	EDP2_TX1-	22	EDP2_TX1+
	23	EDP2_TX2-	24	EDP2_TX2+
	25	GND	26	GND
	27	EDP2_TX3-	28	EDP2_TX3+
	29	EDP2_AUX-	30	EDP2_AUX+

Notes:

[1]: Panel Power VDD is 3.3V by default, 5V is selectable by “eDP2 VDD Select Jumper” (JC_EDP1 Table 19).

21) J2* (Debug Header2 3*1 Pin 2.54mm)

Graphic	Pin	Definition	Pin	Definition
	1	GP3.0_RXD	3	GND
	2	GP3.1_TXD		

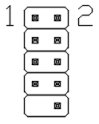
Notes:

[1]: J2 is not onboard by default.

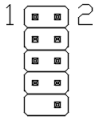
22) EDP_P1 (eDP2 Backlight Control Header 6*1 Pin 2.00mm)

Graphic	Pin	Definition	Pin	Definition
	1	GND	4	EDP2_BKLT_EN
	2	GND	5	+ 12V
	3	EDP2_BKLT_CTL	6	+ 12V

23) F_USB2 (Front USB2.0 Header2 5*2 Pin 2.54mm)

Graphic	Pin	Definition	Pin	Definition
	1	+ 5V	2	+ 5V
	3	HUB1_USB_3-	4	HUB1_USB_4-
	5	HUB1_USB_3+	6	HUB1_USB_4+
	7	GND	8	GND
	9		10	GND

24) F_USB3 (Front USB2.0 Header3 5*2 Pin 2.54mm)

Graphic	Pin	Definition	Pin	Definition
	1	+ 5V	2	+ 5V
	3	HUB1_USB_1-	4	HUB1_USB_2-
	5	HUB1_USB_1+	6	HUB1_USB_2+
	7	GND	8	GND
	9		10	GND

25) F_USB4* (Front USB2.0 Header4 4*1 Pin 2.00mm)

Graphic	Pin	Definition	Pin	Definition
	1	+ 5V	3	USB2_4+ [1]
	2	USB2_4- [1]	4	GND

Notes:

[*]: F_USB4 is not onboard by default.

[1]: F_USB4 colay USB2_4 signal with M.2_KEYB_WWAN1. It supports M.2_KEYB_WWAN1 by default and can support F_USB4 if specified. (resistor selectable)

26) F_USB5 (Front USB2.0 Header5 4*1 Pin 2.00mm)

Graphic	Pin	Definition	Pin	Definition
	1	+ 5V	3	USB2_9+ [1]
	2	USB2_9- [1]	4	GND

Notes:

[1]: F_USB5 colay USB2_9 signal with USB audio codec. It supports F_USB5 by default and can support USB audio codec if specified. (resistor selectable)

27) DC_OUT1 (DC 12V+5V Power Output Header 4*1 Pin 2.54mm)

Graphic	Pin	Definition	Pin	Definition
	1	+ 12V	3	GND
	2	GND	4	+ 5V

28) SYS_FAN1 (System FAN Header 3*1 Pin 2.54mm)

Graphic	Pin	Definition	Pin	Definition
	1	GND	3	FAN Speed Detection2
	2	+ 12V		

29) CPU_FAN1 (CPU FAN Header 4*1 Pin 2.54mm)

Graphic	Pin	Definition	Pin	Definition
	1	GND	3	FAN Speed Detection1
	2	+ 12V	4	FAN Speed Control1

30) J1 (Debug Header1 4*1 Pin 2.00mm)

Graphic	Pin	Definition	Pin	Definition
	1	VCCIN_SDA	3	VCCIN_PE
	2	VCCIN_SCL	4	GND

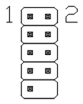
31) CASH1 (Cash Drawer Header 4*1 Pin 2.00mm)

Graphic	Pin	Definition	Pin	Definition
	1	+ 12V	3	Cash Drawer Detect
	2	Cash Drawer Control	4	GND

32) DC_IN2 (DC 12V Power Input Header 4*1 Pin 2.54mm)

Graphic	Pin	Definition	Pin	Definition
	1	+ 12V_IN	3	GND
	2	+ 12V_IN	4	GND

33) J_COM1* (COM1 Header 5*2 Pin 2.00mm)

Graphic	Pin	Definition	Pin	Definition
	1	COM1_PIN1 [1]	2	COM1_RXD
	3	COM1_TXD	4	COM1_DTR#
	5	GND	6	COM1_DSR#
	7	COM1_RTS#	8	COM1_CTS#
	9	COM1_PIN9 [2]	10	

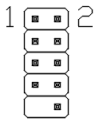
Notes:

[*]: J_COM1 and COM1 share the same signal, they can't be accessed simultaneously. J_COM1 is not onboard by default.

[1]: PIN1 of COM1 can be DCD# (default) /5V/12V, selectable by resistor.

[2]: PIN9 of COM1 can be RI# (default) /5V/12V, selectable by resistor.

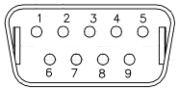
34) F_USB1 (Front USB2.0 Header1 5*2 Pin 2.54mm)

Graphic	Pin	Definition	Pin	Definition
	1	+ 5V	2	+ 5V
	3	USB_5-	4	USB_6-
	5	USB_5+	6	USB_6+
	7	GND	8	GND
			10	GND

Notes:

[1]: F_USB1 colay USB2_5 signal with R_USB1. It supports F_USB1 by default and can support R_USB1 if specified. (resistor selectable)

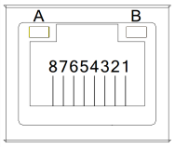
41) COM1* (COM1 DB9/M Connector)

Graphic	Pin	Definition	Pin	Definition
	1	COM1_PIN1 [1]	6	COM1_DSR#
	2	COM1_RXD	7	COM1_RTS#
	3	COM1_TXD	8	COM1_CTS#
	4	COM1_DTR#	9	COM1_PIN9 [2]
	5	GND		

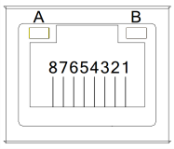
Notes:

[*]: COM1 and J_COM1 share the same signal, they can't be accessed simultaneously.
[1]: PIN1 of COM1 can be DCD# (default) /5V/12V, selectable by resistor.
[2]: PIN9 of COM1 can be RI# (default) /5V/12V, selectable by resistor.

45) RJ45_2 (GBE LAN RJ45 Connector2 8Pin)

Graphic	Pin	Definition		Pin	Definition	
	1	MDI0_2+		5	MDI2_2-	
	2	MDI0_2-		6	MDI1_2-	
	3	MDI1_2+		7	MDI3_2+	
	4	MDI2_2+		8	MDI3_2-	
	A	Active LED	ACT: Twinkling Yellow	B	Speed LED	1000M: Turn Yellow
			Only LINK: Lights Off			100M: Turn Green
			Stop: Lights Off			10M: Lights Off

46) RJ45_1 (GBE LAN RJ45 Connector1 8Pin)

<table>
<tr><th>Graphic</th><th>Pin</th><th colspan="2">Definition</th><th>Pin</th><th colspan="2">Definition</th></tr>
<tr><td rowspan="7"> 
</td><td>1</td><td colspan="2">MDI0_1+</td><td>5</td><td colspan="2">MDI2_1-</td></tr>
<tr><td>2</td><td colspan="2">MDI0_1-</td><td>6</td><td colspan="2">MDI1_1-</td></tr>
<tr><td>3</td><td colspan="2">MDI1_1+</td><td>7</td><td colspan="2">MDI3_1+</td></tr>
<tr><td>4</td><td colspan="2">MDI2_1+</td><td>8</td><td colspan="2">MDI3_1-</td></tr>
<tr><td rowspan="3">A</td><td rowspan="3">Active LED</td><td>ACT: Twinkling Yellow</td><td rowspan="3">B</td><td rowspan="3">Speed LED</td><td>1000M: Turn Yellow</td></tr>
<tr><td>Only LINK: Lights Off</td><td>100M: Turn Green</td></tr>
<tr><td>Stop: Lights Off</td><td>10M: Lights Off</td></tr>
</table>

7. BIOS setup

See “BIOS Spec for SV1a-64126 Series” for detail information of BIOS setup.

【End】